Serial No. 09/893,598
Docket No. 01USFP644-M.K.

## REMARKS

Entry of this Amendment is proper under 37 CFR §1.116, since no new claims or issues are presented by the claim amendments. Indeed, such amendments are made in view of the Examiner's kind and helpful comments in the October 20, 2004, Office Action, which would distinguish over the prior art and overcome the 35 USC § 112, second paragraph, criticisms.

Claims 1-20 are presently pending in this application. Applicant gratefully acknowledges Examiner Bell for taking time to make suggested claim wording changes in the latest Office Action. The claim amendments above reflect some of his helpful suggestions. Applicant's concerns over the remaining suggested changes are described below.

Claims 1-10 and 15-20 stand rejected under 35 USC §112, second paragraph, as indefinite. Claims 1, 2, 10, 15, 16, and 20 stand rejected under 35 USC 102(e) as anticipated by US Patent 5,793,363 to Takuwa.

These rejections are respectfully traversed in the following discussion.

## I. THE CLAIMED INVENTION

As defined by, for example, claim 1, the claimed invention is directed to a semiconductor circuit system including a first signal line and n circuit sections, where n is an integer more than 2, each of which circuit sections includes an input terminal and an output terminal.

The input terminals of only predetermined k ones of the n circuit sections are connected to the first signal line, where k is an integer equal to or greater than 2 and less than n. The output terminal of an $m^{th}$ one of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of the n circuit sections, where m is an integer varying between 1 and n-k.

## II. THE 35 USC §112, SECOND PARAGRAPH, REJECTION

The Examiner rejected claims 1-10 and 15-20 as being indefinite because of conflicts between the various integer ranges. Applicant believes the above claim amendments resolve these conflicts.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Along these lines, Applicant explains why it is considered that not all of the Examiner's suggested claim changes would seem appropriate. First, although the word "variable" might be appropriate during the design phase of a chip, Applicant prefers not to use this term to describe the fixed number of units embedded on an implemented circuit system such as described by the claims. In Applicant's opinion, the term "variable" in the claim language may raise various issues as intended to describe the number of circuit components in a functioning circuit, since the disclosure does not address the feature of varying the number of units in the implemented system described by the claims, as would be implied by the terminology "variable".

Second, although the Examiner has reasonably worked from the exemplary embodiments shown in the figures of the Application, Applicant does not wish to be limited only to these specific examples. Thus, it would seem that the present invention overcomes the prior art of record for $n = 3$, rather than $n = 4$, as suggested by the Examiner.

Finally, the Examiner's suggested final limitation that $n = k \cdot g$ (where g is some integer) would seem to be too limiting, since there is no reason that the number n cannot be a prime number (e.g., 3, 7, 11, 13). If, for example, $n = 3$ and $k = 2$, there is no integer other than 1 for which $n = k \cdot g$.

More important, there is no reason that the total number n be an integral multiple of k, since, for example, if the example shown in Figure 4 had shown $n = 5$, $k = 2$, the technique of having the $m^{th}$ output to be the $(m+k)^{th}$ input is still in effect through $m = n-k$. That is, there is a residual of n-k stages left over for which the output does not become an input for another subsequent stage, but the index m is described in the claim as varying only up through n-k.

Therefore, Applicant respectfully declines to add this limitation to the independent

claims. However, Applicant again gratefully acknowledges the Examiner's efforts in attempting to arrive at appropriate claim language to describe the present invention.

## III. THE PRIOR ART REJECTION

The Examiner alleges that Takuwa teaches the invention of claims 1, 2, 10, 15, 16, and 20. Applicant submits, however, that there are elements of the invention of these claims which are neither taught nor suggested by Takuwa.

More specifically, as can be seen in the example shown in Figure 4 of the present Application in which is exemplarily shown n = 6 and k = 2. As m varies between 1 and 4 (e.g., between 1 and n-k), m + k would vary between 3 and 6, so that the first input signal line 5 connects to the input terminal of circuit sections 2-1,2-2 (e.g., k = 2) and the output terminal of the $m^{th}$ circuit section is connected to the input terminal of the $(m + k)^{th}$ circuit section.

In contrast, in Figure 1 of Takuwa (upon which the Examiner is relying on for allegedly teaching the inventive semiconductor circuit system), if ST is considered to be the input signal port of each circuit section, is connected to the input terminal of the first the first circuit section 1-1a. However, in Takuwa, k = 1, since the output signal "OUTi" is connected to be the input into the next circuit section. Therefore, in this configuration shown in Takuwa Figure 1, n = 3 and k = 1, whereas the present invention defined by the independent claims requires that k be 2 or greater.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Takuwa of: "...wherein said input terminals of only predetermined k ones of said n circuit sections are connected to said first signal line, where k is an integer equal to or greater than 2 and less than n...", as required by claim 1. Independent claims 15 and 20 have similar language.

For this reason, claims 1, 2, 10, 15, 16, and 20 are clearly patentable over Tukuwa.

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## IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

Date: 1/19/2005

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**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that I am filing this Amendment Under 37 C.F.R. §1.116 by facsimile with the United States Patent and Trademark Office addressed to Examiner Paul A. Bell, Group Art Unit 2675, at fax number (703) 872-9306 this 19th day of January, 2005.

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